



Article

Comparison of System-Level Design Approaches on Different Types of Digitally-Controlled Ring-Oscillator †

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Abstract: This paper presents a comparative study between two different implementations of digitally-controlled-oscillators (DCOs), which is the DAC-based and the digital controller-based DCO in TSMC 65 nm CMOS technology. This paper focuses on ring-oscillator architectures due to their high stability against PVT. The DAC-based oscillator implements a differential architecture, and the digital controller-based architecture operates in a single-ended signal. The SFDR of the DAC-based DCO is 77.2 dBc and controller-based DCO is 56.8 dBc at 125 MHz offset. The Monte-Carlo simulation gives a deviation of 7.4 % and 8.5 % for the DAC-based and controller-based DCO, respectively. The phase noise performance of the DAC-based DCO and controller-based DCO is -78.9 dBc/Hz and -81.3 dBc/Hz at 1 MHz offset, respectively. The implementations are given and compared according to their performance based on post-layout simulation results.



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Keywords: digitally-controlled-oscillator (DCO); frequency generation; digital-to-analogue converter (DAC)

1. Introduction

Phase-locked loops (PLLs) are widely implemented in radio, wired and wireless telecommunication, clock generation, and other electronic applications. Because high-performance system-on-chip (SoC) requires multiple simultaneously generated frequencies, several frequency generators need to be implemented in the system. These frequencies can be generated and synchronised by using a PLL. It is a closed-loop system that uses the phase-locking technique to align the output signal phase in phase with the input signal phase.

PLLs are classified into analogue and digital PLLs [1]. Analogue PLLs provide good phase-noise performance and high accuracy with the cost of a large chip size and high power consumption due to the analogue nature of the loop filter [2]. In contrast to an analogue PLL, digital PLLs consume less power and area while compromising linearity, as the generated frequency can only be varied in discrete steps limited by the resolution of the control bits [3]. On the other hand, the digital PLL provides short locking time and strong robustness against process, voltage, and temperature (PVT) changes due to the lack of analogue components [4]. Digital PLL can benefit for the shorter locking time depends on their controller type such as SAR [5]. Because of their larger locking step, they can reach correct locking point faster compared to analogue PLL despite digital PLL suffers from limited resolution. On the other hand, analogue PLL has an infinite resolution, therefore it provides much smaller locking step to achieve correct locking point with smaller phase error compared to digital PLL [6]. At the same time, a digital PLL suffers from several disadvantages in terms of jitter and phase-noise performance when compared to an analogue PLL.

The most crucial part of the digital PLL is the digitally-controlled oscillator (DCO) that generates a periodic signal whose frequency is achieved by digital control input code.

It decides the overall performance, such as phase noise and jitter, tuning range, power consumption, and the total occupied area. In this regard, two common types of DCO exist: LC-based DCOs and ring-oscillator based DCOs. The LC-based DCO gives better phase-noise performance and resolution, but it occupies a larger chip area, consumes more power, and suffers from higher degree of mutual coupling between oscillators. A ring-oscillator based DCO occupies a significantly smaller area and it is less susceptible towards PVT changes. A DCO can be realised in two different approaches, as presented in Figure 1. The first approach, as seen in Figure 1a, is a hybrid approach, where the traditional voltage-controlled oscillator (VCO) is used with a digital-to-analogue converter (DAC) to be integrated with the rest of the digital PLL. The advantage of this system is that the VCO requires a minimal redesign from analogue to digital PLL to adapt to the control voltage that is given by the DAC. However, the performance of these components strongly depends on their analogue behaviour of the DAC, restricting the key advantage of the digital PLL system. The second approach, as shown in Figure 1b, utilises a digital control mechanism for frequency tuning. In inverter-based ring oscillators, inverters that make the ring are classified into addressable components. The frequency is then tuned by increasing or decreasing the effective delay in the inverters. This is achieved by turning on or off the transistors that can tune the total delay time of each cell in the ring oscillator. This paper compares the performance of the DCO that is controlled by the analogue and digital behaviour of the system.

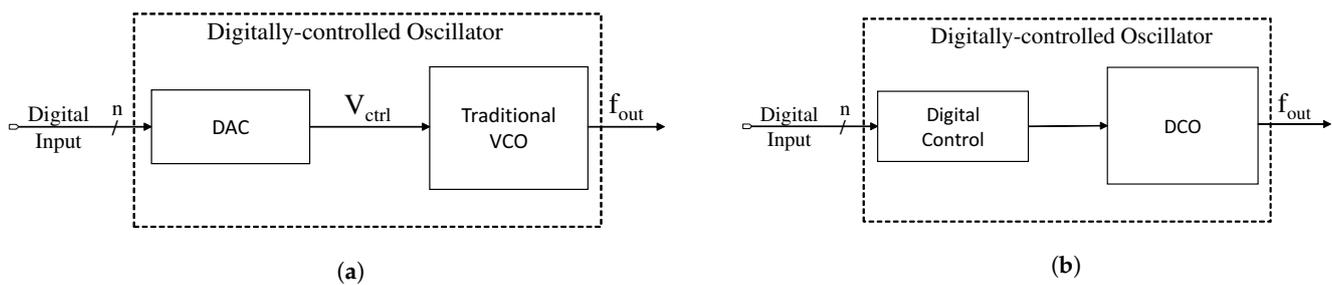


Figure 1. DCO controlled by (a) DAC, and by a (b) digital controller.

The paper is structured, as follows: Section 2 describes the two different implementations for the DCO. The simulation result and comparison of the two implementations are presented in Section 3 and, finally, conclusions are given in Section 4.

2. General DCO Characteristics

2.1. DAC-Based DCO

Figure 2 shows the block diagram of the DAC-based DCO. The four input bits $\langle A, B, C, D \rangle$ are given to the 4×16 one hot coding-based decoder, which then decodes it to 16 control bits. These control bits are fed to the DAC, which tunes the frequency of the VCO accordingly. Alternatively, the input bits can be given directly to the DAC, which increases the resolution of the DCO. The designed DAC controls the delay time in the delay cell by varying the current through the delay cells. This change in current at the charging and discharging nodes produces the variation in oscillation frequency. The current sources occupy a considerably smaller area and consume less power. The output of the oscillator should drive large transistors, hence the output of the oscillator $I+$, $I-$, $Q+$ and $Q-$ are passed on to the corresponding buffers.

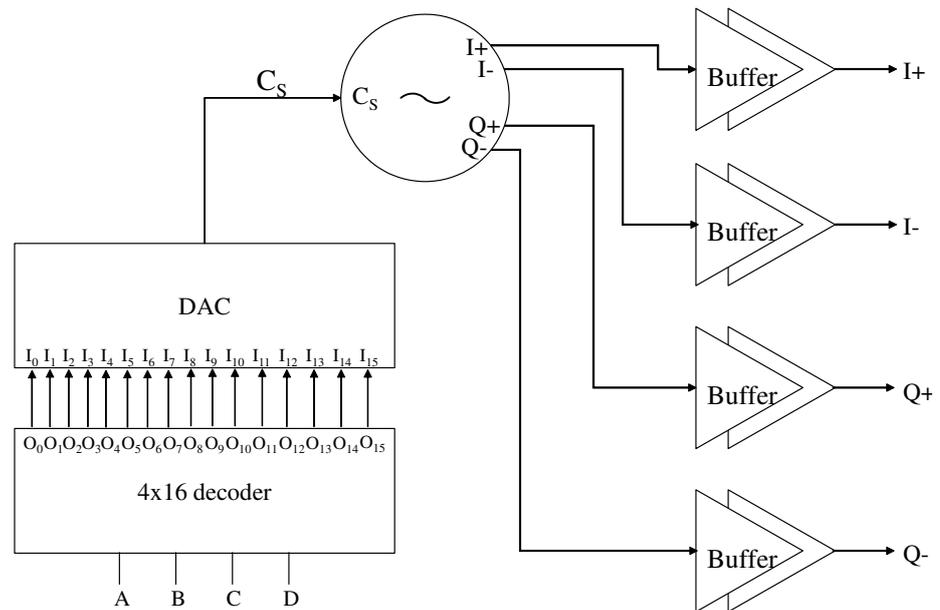


Figure 2. Block diagram of the DAC-based DCO [7].

The DAC-based DCO is designed differentially with four delay cells, which are controlled with the help of a control signal (C_s) from the DAC, as shown in Figure 3a. A cross-coupled architecture is chosen for the delay cell, as it provides better phase noise and jitter performance. The delay from the cross-coupled architecture is regulated by varying the node currents by the C_s . A differential ring-oscillator structure, as shown in Figure 3b, is chosen due to its high stability, strong robust against substrate and supply noise, and its capability to generate in-phase and quadrature signal components.

C_s is derived from the current source, a weighted transistor array, as shown in Figure 4. To obtain linear and fine-tuning of the DCO, the pMOS transistors are arranged in increasing order of their size. The size of the $(n + 1)$ th pMOS transistor is increased by the step of the smallest size of the pMOS transistor. The frequency of oscillation increases as the size of the transistor increases, due to the higher current through the delay cells. C_s is obtained from the nMOS transistor, which is always ON. This keeps the output capacitance of the DAC independent of the weighted pMOS transistors, which helps to change the oscillation frequency linearly. Each pMOS transistor in the DAC can be designed independently, as only one pMOS transistor becomes active at a given time. This grants the freedom to assign custom frequencies to a digital code, by tuning the size of the pMOS transistor. The control bits for the DAC can be directly obtained from the digital loop filter (DLF) or via a decoder. Obtaining the control bits directly from the DLF improves the resolution of the DCO to 6.10 kHz [7].

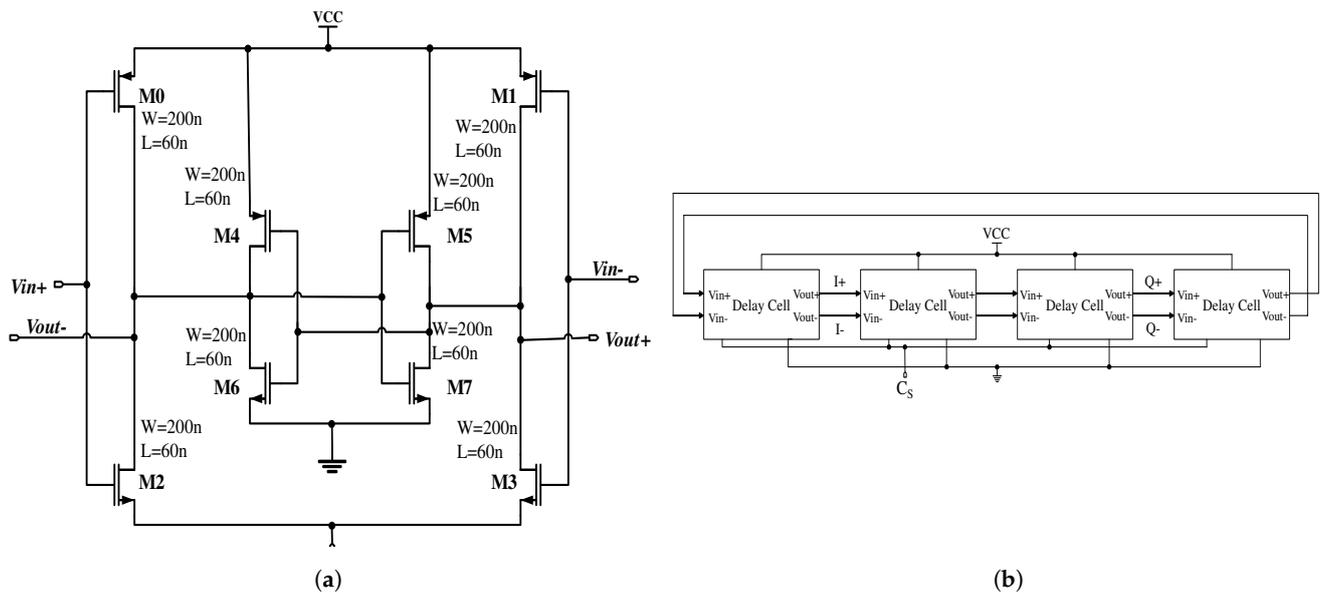


Figure 3. (a) Schematic of delay cell, (b) Block diagram of the ring oscillator [7].

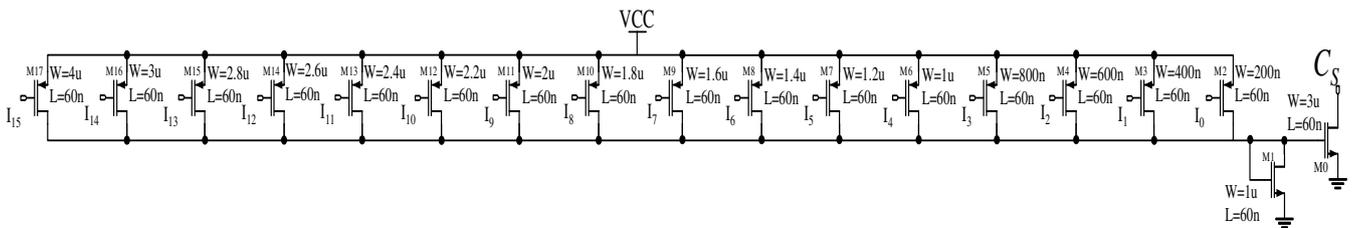


Figure 4. Schematic of the DAC [7].

2.2. Controller-Based DCO

Figure 5 shows the block diagram for the controller-based DCO. The row and column control signals are obtained from the controller and the frequency is tuned accordingly. The dither control signals are acquired from the delta-sigma modulator and they are used for fine-tuning of the DPLL. The three-stage ring oscillator in the proposed design consists of four rows and six columns of CMOS inverters. The schematic of the delay cell is as shown in Figure 6. Each stage of the oscillator is connected in parallel. The frequency of the DCO is tuned by increasing or decreasing the size of the transistors, which changes the charge/discharge current through the transistors. When the size of transistors M0 and M3 increase, the oscillation frequency and frequency tuning range of the DCO increases. The frequency tuning range decreases when the size of M4 and M5 increases, but the oscillation frequency shifts upwards. As more inverters are turned ON, the oscillation frequency of the DCO increases, at the same time as the current driving capability of the inverters increases. The inverter is controlled by the signals from the row control, column control, and row-override blocks. An inverter is turned ON when both row and column-control signals are logic HIGH or the signal row-override signal is logic HIGH.

The rows and columns of the oscillator are adjusted by the digital controller, as illustrated in Figure 7. The controller receives the SIGN signal as input, based on which the counter starts counting up or down. The SIGN signal is obtained from the PFD, which transmits the information whether the reference signal is leading or lagging. The input CLK signal is the delayed version of the reference signal. The EN_{FINE} signal controls the counter and register clock. These blocks only operate when the EN_{FINE} signal is logic LOW. The register clock block generates two clocks, CLK_{MAX} and CLK_{MIN} signals based on the SIGN, CLK_{REF} and EN_{FINE} signals. Based on these clocks, the register block stores the last two maximum and minimum values of the output states of the counter. These values are

then passed on to the control check block. This block verifies whether the two maximum and minimum values are close enough. In the proposed design, the threshold is set to 2, which is, if the difference between the maximum or the minimum values stored is less than or equal to 2, then the signal EN_{FINE} is set HIGH. Additionally, the control check block loads the average of the last maximum and minimum value to the multiplexer. The EN_{FINE} signal toggles the multiplexer output and disables the clock to the counter and the register clock block, thus enabling the fine-tuning for DPLL. The LSB signals from the multiplexer are transmitted to the column-control block and the MSB signals to the row-control block. These blocks are identical digital blocks, which select the row and column of the DCO according to the multiplexer output.

When the counter increases by one, the controller turns ON one more delay cell, which is shown in Figure 6, from the same partially turned ON row. After all inverters in the current row are turned ON, then the first inverter in the next row is turned ON. That is, when the column reaches its maximum, then the column resets to its first column and the row increases by one. Similarly, when the counter decreases by one, the counters acts in the reverse direction. In the proposed design, the oscillator oscillates between 5.252 GHz and 6.344 GHz with 25 steps. The gain of the DCO is 48 MHz/LSB.

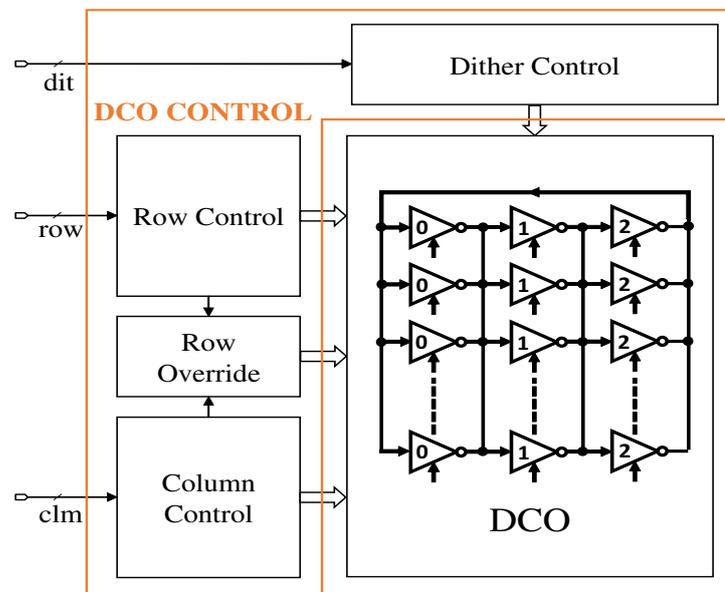


Figure 5. Block diagram of controller-based DCO.

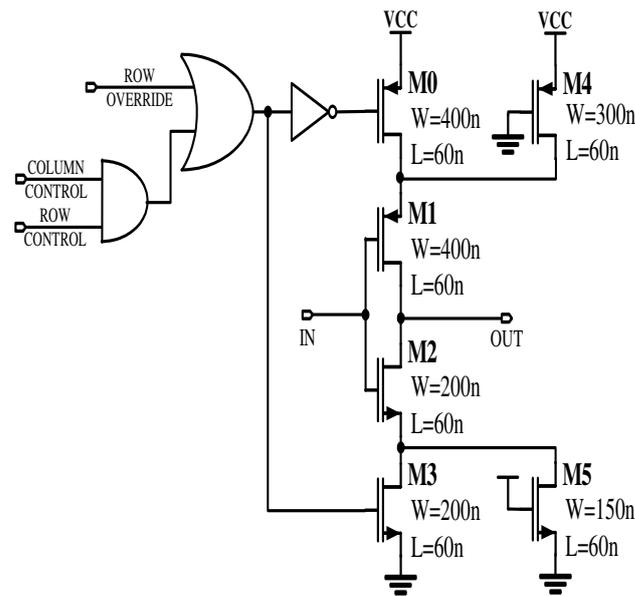


Figure 6. Schematic of the delay cell.

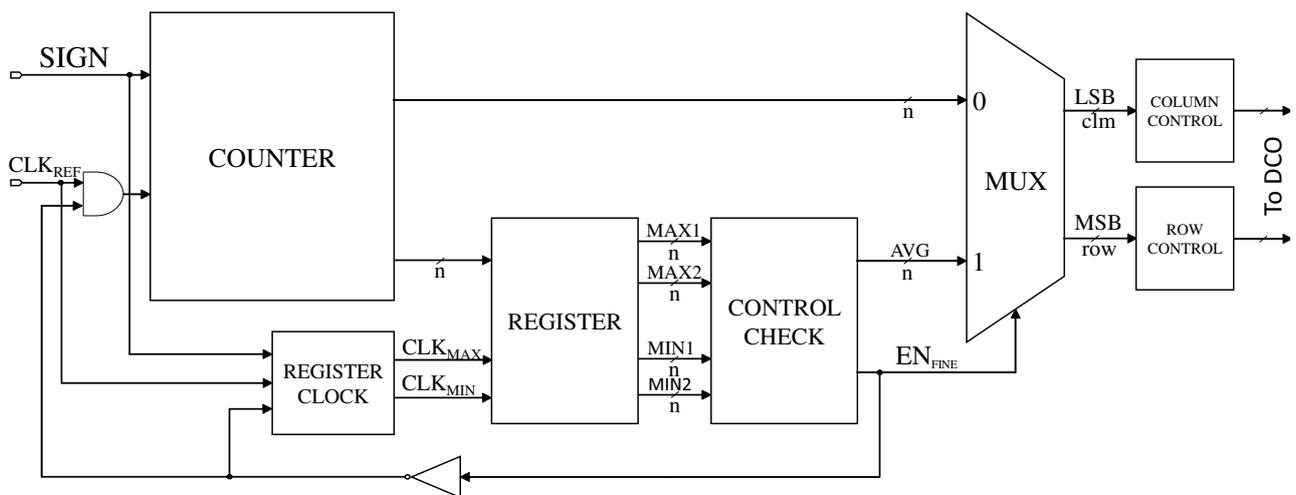


Figure 7. Block diagram of the controller.

3. Layout and Simulation Results

The layouts of the DAC-based DCO and the controller-based DCO with an area of $36.33 \mu\text{m}^2$ and $550 \mu\text{m}^2$ in TSMC 65 nm CMOS technology, respectively, are shown in Figure 8. The blank space on the top in the controller-based DCO can be used for implementing the dither control, which makes the layout more compact. All of the simulations are performed with extracted RC parasitics from the layout. Whereas, the DAC-based differential ring oscillator oscillates between 1.8 GHz and 2.2 GHz, consuming an average power of 1.6 mW. The designed controller-based DCO operates between 5.2 GHz and 6.4 GHz, and it consumes an average power of 2.5 mW. Both of the oscillators operates from 1.2 V and the power is measured with the oscillators running at their highest frequency along with their control circuit and the buffers.

Figure 9 shows the phase noise characteristics of the free running oscillator in both types. The phase noise performance can be improved by using the DCO in a closed-loop system with proper loop filter adjustment. The phase noise of the DAC-based DCO and controller-based DCO at 2.2 GHz and 6.4 GHz is -78.9 dBc/Hz and -81.3 dBc/Hz at 1 MHz offset,

respectively. The jitter performance of the DCOs is measured from the eye diagram at their highest operating frequency. The peak-to-peak jitter obtained for the DAC-based DCO is 8.7 ps and for the controller-based DCO is 6.8 ps at 2.2 GHz and 6.4 GHz, respectively, as shown in Figure 10. The spectrum of the DAC-based DAC at 2.2 GHz and controller-based DCO at 6.34 GHz is shown in Figure 11. The spectrum is a measure of distortions to the signal by other noise sources. The Spurious Free Dynamic Range (SFDR) of the DAC-based and controller-based DCO at 125 MHz is 77.2 dBc and 56.8 dBc, respectively. DAC-based and controller-based DCOs both show a linear behaviour with increase in input control bits. Monte Carlo simulations are performed for both the DAC-based and controller-based DCOs, and the deviation of 7.4% and 8.5% was observed in the output frequency.

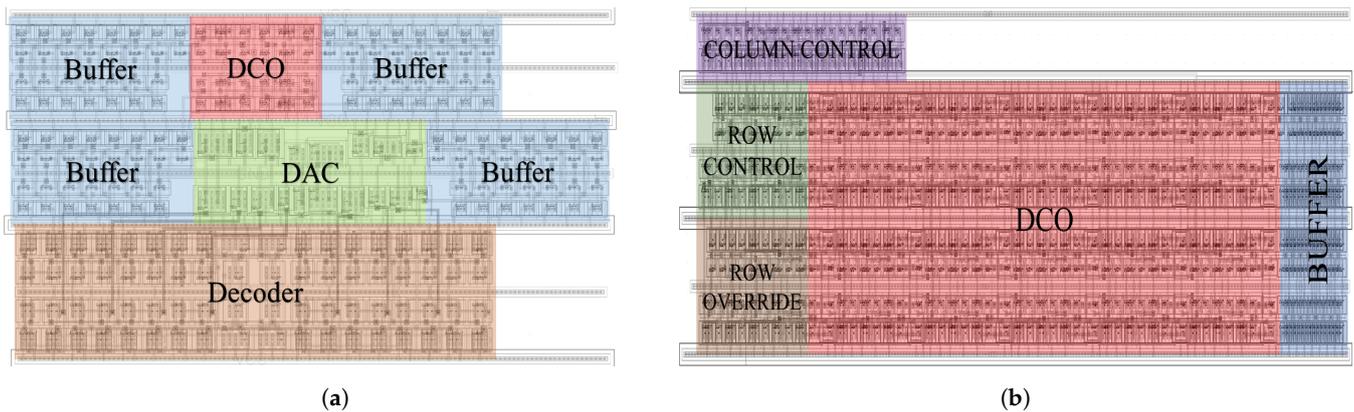


Figure 8. Layout of the (a) DAC-based DCO, (b) Controller-based DCO.

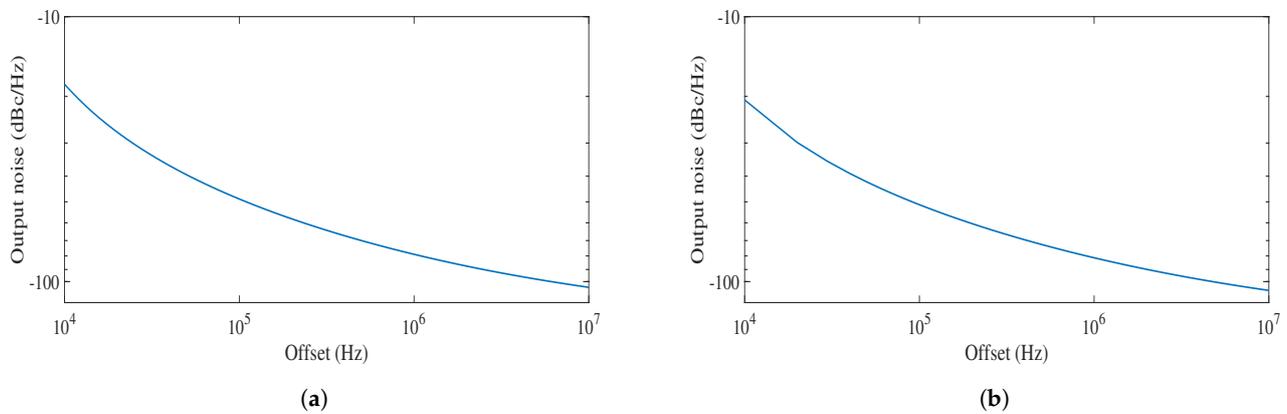


Figure 9. Phase noise performance of the (a) DAC-based DCO, (b) Controller-based DCO.

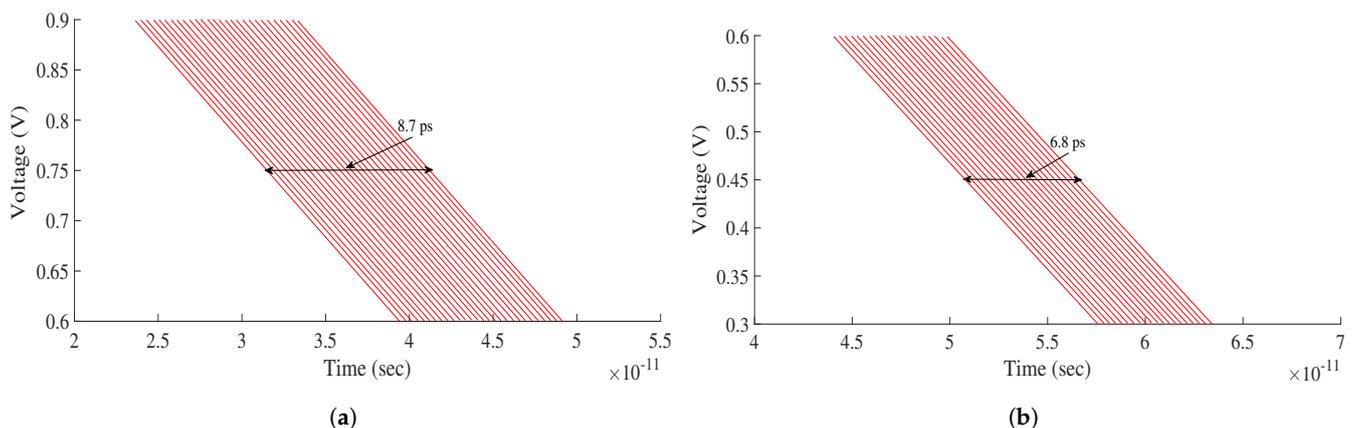


Figure 10. Jitter of the (a) DAC-based DCO at 2.2 GHz, (b) Controller-based DCO at 6.4 GHz.

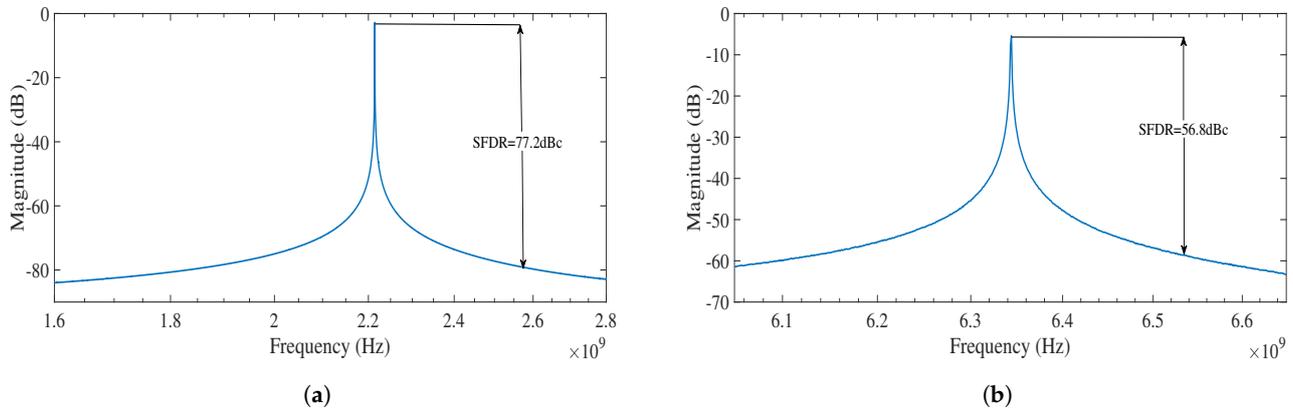


Figure 11. Spectrum of the (a) DAC-based DCO at 2.2 GHz, (b) Controller-based DCO at 6.4 GHz.

Table 1 shows a comparison with state-of-the-art ADPLL. The DAC-based DCO and controller-based DCO outperform the state-of-the-art designs in terms of area and power consumption. The implemented DAC-based DCO gives an advantage in terms of the resolution and step size of the frequency shifting of the ring oscillator due to the analogue behaviour of the design. On the other hand, the proposed design may suffer from the process variation since the size relation between current charging transistors in the DAC directly affect the analogue output control voltage that changes based on digital input data. The second implementation which is the fully digital controller-based DCO does not require any precise current charging capability. Thus, the process variation can have a less effect on the working principle of the proposed controller. Additionally, since this locking step primarily controlled by the SIGN signal generated by a conventional phase detector, the robustness of the controller is further improved against process variation as compared to the conventional time-to-digital converter (TDC) based controller, which makes them sensitive to the any changes in resolution. The Figure-of-Merit for jitter (FOM_{jitter}) of the DAC-based and controller-based DCO outperform [8], and they are almost the same with [9]. The [10] is based on the schematic simulation, hence the FOM_{jitter} is better than the proposed designs. The DCO in [11] is designed using 28 nm technology and it uses LC-tank based architecture. Hence, the phase noise performance of [11] is better than the DAC-based and controller-based DCO. However, its active area is much larger than the proposed DAC-based and controller-based DCO in spite of the DCO that was implemented in 28 nm. The DAC-based DCO and controller-based DCO outperform [8,9] in terms of peak-to-peak jitter performance. The proposed design uses a simple architecture and it occupies a less active area. Hence, for SoC applications where multiple PLLs are required, the introduced locking techniques, especially the fully digital controller-based DCO, occupy smaller active with comparable performance compared to state-of-the-art designs.

Table 1. Performance Summary and comparison with state-of-the-art.

	This Work (DAC-Based)	This Work (Controller-Based)	[10] ¹	[11] ²	[8]	[9]
Technology (nm)	65	65	65	28	180	55
Tuning Range (MHz)	400	1200	1900	730	800	2450
Phase Noise (dBc/Hz)	−78.9 @1 MHz	−81.3 @1 MHz	-	−109.5 @1 MHz	-	-
Peak-to-Peak Jitter (ps)	8.7 @2.2 GHz	6.8 @6.4 GHz	6.47 @2.7 GHz	-	22.3 @1.28 GHz	9.6 @2.7 GHz
VDD (V)	1.2	1.2	1.2	0.8	1.8	-
Power (mW)	1.6 ³	2.5 ³	1	0.35	22.68	1.103
Active Area (mm ²)	0.00037	0.00550	-	0.042	0.053	0.0129
Figure of Merit ⁴ (FOM) (dB)	−219.2	−219.4	−223.8	-	−199.5	−220

¹ Simulation result without extracted parasitics; ² LC Tank based DCO; ³ It is the total power consumed by ring oscillator, control circuit and buffers; ⁴ $FOM_{\text{jitter}} = 10 \log_{10} \left\{ \left(\frac{\sigma^2}{f_s} \right) \left(\frac{P_{\text{DC}}}{P_{\text{mW}}} \right) \right\}$.

4. Conclusions

A DAC-based DCO and controller-based DCO are designed using TSMC 65 nm CMOS technology. The DAC-based DCO is designed with four digitally-controlled differential stages leading to a tuning range from 1.8 GHz to 2.2 GHz. The controller-based DCO is designed with three digitally-controlled stages that can be tuned from 5.2 GHz to 6.4 GHz. The DAC-based DCO provides better resolution than the controller-based DCO, as the DAC-based architecture is analogue in nature. However, the resolution of the controller-based architecture can be increased by adding dithering stages controlled by a delta-sigma modulator. For both architectures, the layout is constructed, verified with DRS and LVS, and the parasitic components of the layout version are extracted. The designs are checked for their phase noise performance, peak-to-peak distortions, and for their jitter performance. The designs are small in size and are linear in nature.

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